



IPW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Bruno GHYSELEN *et al.* Confirmation No.: 8095
Application No.: 10/615,259 Group Art Unit: 2818
Filing Date: July 9, 2003 Examiner: Thao P. Le
For: PROCESS FOR TRANSFERRING A Attorney Docket No.: 4717-7500
LAYER OF STRAINED
SEMICONDUCTOR MATERIAL

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Pursuant to Applicant's duty of disclosure under 37 C.F.R. § 1.56, enclosed is a Form PTO-1449 listing twelve (12) references for the Examiner's review. References C1 and C3 were published prior to the filing of the present application.

Copies of references B1-B5 and C1-C3 are enclosed herewith. Also enclosed is a copy of the International Search Report from the corresponding PCT application. Copies of U.S. patent references A1-A4 will be provided if the Examiner so requests.

It is respectfully requested that the references be made of record in this application by the Examiner's completion and return of the attached Form PTO-1449.

No fee is believed to be due for the submission of the these references. Should any fees be required, however, please charge such fees to Winston & Strawn LLP Deposit Account No. 50-1814.

Respectfully submitted,

May 28, 2004
Date

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WINSTON & STRAWN LLP
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202-371-5771

LIST OF REFERENCES CITED BY APPLICANT

Form PTO-1449

(Use several sheets if necessary)

ATTY. DOCKET NO.:

4717-7500

APPLICATION NO.:

10/615,259

APPLICANT:

Bruno GHYSELEN et al.

MAY 28 2004

Sheet 1 of 1

FILING DATE:

July 9, 2003

GROUP:

2812

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	CITE NO.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	A1	6,524,935	02/2003	Canaperi et al	438	478	
	A2	2003/0089901	05/2003	Fitzgerald	257	19	
	A3	6,603,156	09/2003	Rim	257	190	
	A4	6,737,670	05/2004	Cheng, Zhi-Yuan	257	19	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	B1	2001168342	6/2001	JP				
	B2	WO 02/15244	02/2002	WO				
	B3	WO 02/27783	04/2002	WO				
	B4	WO 02/071493	09/2002	WO				
	B5	WO 02/080241	10/2002	WO				

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

C1	Hobart, K.D. et al., <i>On Scaling the Thin Film Si Thickness of SOI Substrates, A Perspective on Wafer Bonding for Thin Film Devices</i> , Naval Research Laboratory, Electronics Science and Technology division Washington, DC 20375
C2	Mizuno, T. et al., <i>High Performance Strained-Si p-MOSFETs on SiGe-on-Insulator Substrates Fabricated by SIMO Technology</i> , Electron Devices Meeting , 1999. IEDM Technical Digest International, Washington, DC, USA 5-8 December 1999, Piscataway, NJ
C3	Tong, Q. Y. et al., <i>Semiconductor on Wafer Bonding</i> , Science and Technology, Interscience Technology, Johnson Wiley & Sons, Inc.

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.